CLAIMS

1. A receiver circuit comprising:
   - an optical reception device; and
   - an amplifier connected to the reception device, wherein the amplifier includes:
   - a circuit for setting the operating point of the amplifier, and also
   - at least one control terminal of the circuit, by which an operating point of the amplifier can be changed between at least two values at the user end.

2. The receiver circuit as claimed in Claim 1, wherein the amplifier further includes an input transistor, and wherein the circuit for setting the operating point of the amplifier includes means for setting an operating point of the input transistor.

3. The receiver circuit as claimed in Claim 2, wherein the circuit for setting the operating point of the amplifier includes means for forming a setting of the operating point of the input transistor by setting a current in the input transistor.

4. The receiver circuit as claimed in Claim 3, wherein the circuit for setting the operating point of the amplifier is coupled between the input transistor and a reference point, at which the operating voltage is present.

5. The receiver circuit as claimed in Claim 3, wherein the circuit for setting the operating point of the amplifier comprises an impedance network with at least one switching device, which can be changed over by a control signal applied to the at least one control terminal, thereby altering the total impedance of the impedance network.

6. The receiver circuit as claimed in claim 5, wherein the impedance network includes a plurality of ohmic resistors which can be connected in and disconnected by means of the at least one switching device and the at least one control terminal.

7. The receiver circuit as claimed in claim 6, wherein the switching device comprising a switching transistor.

8. The receiver circuit as claimed in claim 1, wherein the amplifier further comprises at least one gain control terminal, by which the gain of the amplifier can be changed over at least between two gain values at the user end.

9. The receiver circuit as claimed in claim 8, wherein the amplifier comprises a transimpedance amplifier.

10. The receiver circuit as claimed in claim 9, wherein the amplifier includes a feedback impedance, which influences the gain of the amplifier.

11. The receiver circuit as claimed in claim 10, it being possible for the impedance of the feedback impedance to be set at the user end by means of the at least one gain control terminal.

12. The receiver circuit as claimed in claim 11, it being possible for the resistance of the feedback impedance to be set at the user end by means of the at least one gain control terminal.

13. The receiver circuit as claimed in claim 10, wherein the feedback impedance comprises an impedance network including at least one switching device, which can be changed

over at the user end by the at least one gain control terminal and which alters the impedance of the feedback impedance in the event of changeover.

14. The receiver circuit as claimed in claim 13, wherein the switching device comprises a switching transistor.

15. The receiver circuit as claimed in claim 10, wherein the feedback impedance comprises an impedance network including at least one variable impedance, the impedance of which can be set within a predetermined impedance range at least approximately linearly at the user end by means of the gain control terminal.

16. The receiver circuit as claimed in claim 15, wherein the variable impedance comprises a transistor.

17. The receiver circuit as claimed in claim 1, further comprising a photodiode.

18. A receiver circuit comprising:

an optical reception device for generating a data signal in response to a received optical signal;

an amplifier circuit comprising:

a first transistor having a control terminal connected to receive the data signal from the optical reception device, a first terminal coupled to ground, and a second terminal,

a second transistor having a control terminal connected to the second terminal of the first transistor, a first terminal coupled to the control terminal of the first transistor, and a second terminal coupled to an operating voltage source,

a first configurable impedance network connected between the control terminal of the first transistor and the second terminal of the second transistor, and

a second configurable impedance network connected between the operating voltage source and the second terminal of the first transistor; and

means for controlling the first and second configurable impedance networks such that, in a first operating mode, the first configurable impedance network generates a relatively high impedance and the second configurable impedance network generates a relatively low impedance, and in a second operating mode, the first configurable impedance network generates a relatively low impedance and the second configurable impedance network generates a relatively high impedance.

19. The receiver circuit according to Claim 18, wherein the first configurable impedance network comprises:

a first terminal connected to the second terminal of the second transistor;

a second terminal connected to the control terminal of the first transistor;

a first impedance element connected between the first and second terminals; and

a second impedance element and a pass transistor connected in series between the first and second terminals, and

wherein said controlling means comprises means for selectively turning off the pass transistor during the

first operating mode, and for turning on the pass transistor during the second operating mode.

20. The receiver circuit according to Claim 18, wherein the second configurable impedance network comprises:

a first impedance element connected between the operating voltage source and the second terminal of the first transistor; and

a second impedance element and a pass transistor connected in series between the operating voltage source and the second terminal of the first transistor, and

wherein said controlling means comprises means for selectively turning on the pass transistor during the first operating mode, and for turning off the pass transistor during the second operating mode.

21. The receiver circuit according to Claim 18, wherein the amplifier circuit further comprises a mirror circuit connected between the first terminal of the second transistor and ground.